WHAT IS CLAIMED IS:

1. A thin-film transistor array of pixels comprising:

a first thin-film transistor including a channel, the channel defined by a region between a first electrode and a second electrode, the channel having a defined length and width;

a pixel addressed by the first thin-film transistor, the pixel having two pixel dimensions including a pixel width and a pixel length, the channel width longer than the shorter of the two pixel dimensions.

2. The thin-film transistor array of claim 1 wherein the ratio of the channel width to the channel length exceeds 5.

3. The thin film transistor array of claim 1 wherein the pixel width is equal to the pixel length.

4. The thin film transistor array of claim 1 wherein the channel includes at least one bend.

5. The thin film transistor array of claim 1 wherein the channel includes at least two bends such that a section of an electrode is surrounded on three sides by the channel in a U configuration.

6. The thin film transistor array of claim 1 wherein the channel completely surrounds one electrode.

7. The thin-film transistor array of claim 1 wherein the semiconductor used in the first thin-film transistor is an organic semiconductor.

8. The thin-film transistor array of claim 1 wherein the semiconductor used in the first thin-film transistor is a polymeric semiconductor.

9. The thin-film transistor array of claim 1 wherein the semiconductor is a continuous film over the array.

10. The thin film transistor array of claim 5 wherein the electrode is the drain electrode.

11. The thin-film transistor array of claim 1 wherein the pixel is backlit liquid crystal material.

12. The thin-film transistor array of claim 1 further comprising:

a gate line coupled to a gate electrode of the first thin film transistor; and,

a second thin film transistor including a corresponding gate electrode coupled to the gate line.

13. The thin film transistor array of claim 1 wherein the channel surrounds a drain electrode.

14. The thin film transistor array of claim 1 wherein the channel includes a first side and a second side, the first side of the channel coupled to the first electrode, the second side of the channel coupled to the second electrode.

15. The thin film transistor array of claim 1 wherein the first electrode is a drain and the second electrode is a source.

16. The thin film transistor of claim 14 wherein the channel includes a top surface, the top surface couples to a third electrode.

17. The thin film transistor of claim 16 wherein the third electrode is a gate.

18. The thin-film transistor array of claim 1 wherein the channel completely surrounds a source electrode.

19. The thin-film transistor array of claim 15 further comprising:

a first data line coupled to a source electrode of the first thin film transistor.

20. The thin-film transistor array of claim 19 further comprising:

a second thin film transistor to address a second pixel, the first data line coupled to a source electrode of the second thin film transistor.

21. The thin film transistor array of claim 20 further comprising:

a second pixel addressed by the second thin film transistor, the second pixel having two dimensions including a second pixel length and a second pixel width, a channel width of the second thin film transistor greater than the smallest dimension of the second pixel.

22. The thin-film transistor array of claim 1 wherein the mobility of a semiconductor used to form the thin film transistor is below 0.5 cm2/Volt-second.

23. The thin-film transistor array of claim 1 further comprising:

a first gate line coupled to a gate electrode of the first thin-film transistor;

a second gate line coupled to a gate of a second thin-film transistor, the second-thin film transistor coupled to a second pixel; and,

a third gate line coupled to a gate electrode of a third thin-film transistor, the third-thin film transistor coupled to a third pixel.

24. The thin-film transistor array of claim 23 further comprising:

a drive circuit coupled to corresponding gate lines of each thin-film transistor, the drive circuit to switch each thin-film transistor to create a pattern in a display.

25. The thin-film transistor array of claim 23 further comprising:

a sensing circuit coupled to each gate line to sense the output of each thin-film transistor in a sensor system.

26. The thin film transistor array of claim 1 wherein the channel width to length ratio exceeds 50.

27. A display device comprising:

a plurality of gate lines;

a plurality of data lines;

a plurality of pixels, each pixel having a two dimensions including a corresponding pixel width and a corresponding pixel length; and,

a plurality of thin film transistors, each thin film transistor to address a corresponding pixel, each thin film transistor in the plurality of thin film transistors including a channel with a channel width, each channel width larger than the smallest dimension of the corresponding pixel addressed.

28. The display device of claim 27 wherein the semiconductor forming the active region of each thin film transistor has mobility less than $0.5cm^2$/Volt-second.

29. The display device of claim 28 wherein the semiconductor is polymeric semiconductor.

30. The display device of claim 28 wherein the semiconductor is an organic semiconductor.

31. The display device of claim 27 further comprising:

an electronic circuit coupled to the plurality of gate lines and the plurality of drain lines, the electronic circuit to individually address each thin film transistor in the plurality of thin film transistors and to individually switch each transistor in the plurality of transistors to display an image.

32. The display device of claim 27 wherein the pixel pad is made from a transparent material to increase the aperture of the pixel.